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-- Company:

-- Engineer:

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-- Create Date: 15:03:39 01/28/2014

-- Design Name:

-- Module Name: four\_digits\_unit - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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**library** IEEE**;**

**use** IEEE**.**STD\_LOGIC\_1164**.ALL;**

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

**use** IEEE**.**NUMERIC\_STD**.ALL;**

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

**entity** four\_digits **is**

**Port** **(**D0**,** D1**,** D2**,** D3 **:** **in** UNSIGNED **(**3 **downto** 0**);**

CK **:** **in** STD\_LOGIC**;**

DP **:** **out** STD\_LOGIC**;**

CATHODES **:** **out** STD\_LOGIC\_VECTOR **(**6 **downto** 0**);**

ANODES **:** **out** STD\_LOGIC\_VECTOR **(**3 **downto** 0**));**

**end** four\_digits**;**

**architecture** Behavioral **of** four\_digits **is**

**signal** DIGIT **:** UNSIGNED **(**3 **downto** 0**);**

**signal** cnt **:** UNSIGNED **(**1 **downto** 0**);**

**begin**

one\_digit\_unit **:** **entity** one\_digit**(**Behavioral**)**

**port** **map** **(**DIGIT **=>** DIGIT**,**

CATHODES **=>** CATHODES**);**

-- one\_digit\_unit calling.

**PROCESS**

**BEGIN**

**WAIT** **UNTIL** **RISING\_EDGE(**CK**);**

cnt **<=** cnt **+** 1**;**

**END** **PROCESS;**

-- Button Pressed

**PROCESS**

**BEGIN**

**CASE** cnt **IS**

**WHEN** "00" **=>**

DIGIT **<=** D0**;** ANODES **<=** "1110"**;** DP **<=** '1'**;**

**WHEN** "01" **=>**

DIGIT **<=** D1**;** ANODES **<=** "1101"**;** DP **<=** '1'**;**

**WHEN** "10" **=>**

DIGIT **<=** D2**;** ANODES **<=** "1011"**;** DP **<=** '0'**;**

**WHEN** **OTHERS** **=>**

DIGIT **<=** D3**;** ANODES **<=** "0111"**;** DP **<=** '1'**;**

**END** **CASE;**

**END** **PROCESS;**

-- Display

**end** Behavioral**;**